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<u>L22</u>	11 and 110	8	<u>L22</u>
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<u>L20</u>	L18 and 110	7	<u>L20</u>
<u>L19</u>	L18 and 19	0	<u>L19</u>
<u>L18</u>	L1 and (laten\$3 or delay\$3 or wait\$3)	305	<u>L18</u>
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<u>L17</u>	18 and 111	5	<u>L17</u>
<u>L16</u>	18 and 110	5	<u>L16</u>
<u>L15</u>	18 and 19	0	<u>L15</u>
<u>L14</u>	18 and 16	4	<u>L14</u>
<u>L13</u>	18 and 15	11	<u>L13</u>

<u>L12</u> 18 and 14	21	<u>L12</u>
<u>L11</u> (712/31)[CCLS]	83	<u>L11</u>
<u>L10</u> (712/31)![CCLS]	83	<u>L10</u>
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<u>L7</u> L1 and (halt\$3 or suspend\$4 or inhibit\$3 or lock\$3)	224	<u>L7</u>
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<u>L5</u> (712/23-37)![CCLS]	2636	<u>L5</u>
<u>L4</u> (712/2-300)[CCLS]	11414	<u>L4</u>
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<u>L2</u> L1 and (halt\$3 or suspend\$4 or inhibit\$3)	163	<u>L2</u>
<u>L1</u> Master\$1 near18 slave\$1 near35 (common\$2 or shar\$6) near4 (memor\$4 or stor\$5)	580	<u>L1</u>

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IEEE CNF IEEE Conference Proceeding

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IEEE STD IEEE Standard

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**1. Multiprocessor shared-memory information exchange**

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Volume 36, Issue 1, Part 1, Feb. 1989 Page(s):626 - 633
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- 9. A VHDL approach to system design for multiprocessor circuit simulation**
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